1. A method to form shallow trench isolations in the manufacture of an integrated circuit device comprising:

providing a silicon semiconductor substrate;

depositing a silicon nitride layer overlying said silicon semiconductor substrate;

depositing a polysilicon layer overlying said silicon nitride layer;

depositing an oxidation mask overlying said polysilicon layer;

patterning said oxidation mask, said polysilicon layer, said silicon nitride layer, and said silicon semiconductor substrate to form trenches for planned shallow trench isolations;

oxidizing said silicon semiconductor substrate exposed within said trenches to form an oxide liner layer within said trenches wherein said oxidation mask prevents oxidation of said polysilicon layer;

removing said oxidation mask;

depositing a trench oxide layer overlying said oxide liner layer and filling said trenches; and

polishing down said trench oxide layer and said polysilicon layer stopping at said silicon nitride layer to complete said shallow trench isolations in the manufacture of said integrated circuit device.

2. The method according to Claim 1 further comprising forming a pad oxide layer having a thickness of between about 80 and 200 Angstroms underlying said silicon nitride layer.

3. The method according to Claim 1 wherein said silicon nitride layer is deposited by chemical vapor deposition to a thickness of between about 800 and 2000 Angstroms.

4. The method according to Claim 1 wherein said polysilicon layer is deposited to a thickness of between about 500 and 1000 Angstroms.

5. The method according to Claim 1 wherein said oxidation mask comprises silicon nitride deposited by chemical vapor deposition to a thickness of between about 200 and 800 Angstroms.

6. The method according to Claim 1 wherein said step of oxidizing said silicon semiconductor substrate forms said liner oxide layer having a thickness of between about 100 and 300 Angstroms.

7. The method according to Claim 1 wherein said step of removing said oxidation mask comprises a wet etch before

said step of depositing said trench oxide layer.

8. The method according to Claim 1 wherein said oxidation mask is removed during said polishing down process.

9. The method according to Claim 1 wherein said step of depositing said trench oxide layer comprises high density plasma chemical vapor deposition (HDP-CVD) of silicon oxide.

10. The method according to Claim 1 wherein said polishing down is performed by a chemical mechanical polishing.

11. The method according to Claim 10 wherein said chemical mechanical polishing uses a polishing slurry having a polishing selectivity of oxide to polysilicon to nitride of 4:100:1.

12. The method according to Claim 1 wherein said trench oxide layer takes on a concave formation when said polysilicon layer is polished and wherein after said all of said polysilicon layer is removed an overpolishing flattens said trench oxide layer.

13. The method according to Claim 10 wherein said chemical mechanical polishing uses a slurry comprising one of the group of: the combination of $NH_4OH$, silica abrasive, and de-ionized water and the combination of potassium hydroxide, silica abrasive, and de-ionized water; and wherein said chemical mechanical polishing process pad comprises polyurethane.

14. A method to form shallow trench isolations in the manufacture of an integrated circuit device comprising:

providing a silicon semiconductor substrate;

forming a pad oxide layer overlying said silicon semiconductor substrate;

depositing a silicon nitride layer overlying said pad oxide layer;

depositing a polysilicon layer overlying said silicon nitride layer;

depositing an oxidation mask overlying said polysilicon layer;

patterning said oxidation mask, said polysilicon layer, said silicon nitride layer, said pad oxide layer, and said silicon semiconductor substrate to form trenches for planned shallow trench isolations;

oxidizing said silicon semiconductor substrate exposed within said trenches to form an oxide liner

layer within said trenches wherein said oxidation mask prevents oxidation of said polysilicon layer;

removing said oxidation mask;

depositing a trench oxide layer overlying said liner oxide layer and filling said trenches; and

polishing down said trench oxide layer and said polysilicon layer stopping at said silicon nitride layer wherein said polishing down is by a chemical mechanical polish using a polishing slurry having a polishing selectivity of oxide to polysilicon to nitride of 4:100:1 to complete said shallow trench isolations in the manufacture of said integrated circuit device

15. The method according to Claim 14 wherein said silicon nitride layer is deposited by chemical vapor deposition to a thickness of between about 800 and 2000 Angstroms.

16. The method according to Claim 14 wherein said polysilicon layer is deposited to a thickness of between about 500 and 1000 Angstroms.

17. The method according to Claim 14 wherein said oxidation mask comprises silicon nitride deposited by chemical vapor deposition to a thickness of between

about 200 and 800 Angstroms.

18. The method according to Claim 14 wherein said step of oxidizing said silicon semiconductor substrate forms said liner oxide layer having a thickness of between about 100 and 300 Angstroms.

19. The method according to Claim 14 wherein said step of removing said oxidation mask comprises a wet etch before said step of depositing said trench oxide layer.

20. The method according to Claim 14 wherein said oxidation mask is removed during said polishing down process.

21. The method according to Claim 14 wherein said step of depositing said trench oxide layer comprises high density plasma chemical vapor deposition (HDP-CVD) of silicon oxide.

22. The method according to Claim 14 wherein said trench oxide layer takes on a concave formation when said polysilicon layer is polished and wherein after said all of said polysilicon layer is removed an overpolishing flattens said trench oxide layer.

23. The method according to Claim 14 wherein said chemical mechanical polishing uses a slurry comprising one of the group of: the combination of $NH_4OH$, silica abrasive, and de-ionized water and the combination of potassium hydroxide, silica abrasive, and de-ionized water; and wherein said chemical mechanical polishing process pad comprises polyurethane.

24. A method to form shallow trench isolations in the manufacture of an integrated circuit device comprising:

providing a silicon semiconductor substrate;

forming a pad oxide layer overlying said silicon semiconductor substrate;

depositing a silicon nitride layer overlying said pad oxide layer;

depositing a polysilicon layer overlying said silicon nitride layer;

depositing an oxidation mask overlying said polysilicon layer;

patterning said oxidation mask, said polysilicon layer, said silicon nitride layer, said pad oxide layer, and said silicon semiconductor substrate to form trenches for planned shallow trench isolations;

oxidizing said silicon semiconductor substrate exposed within said trenches to form an oxide liner

layer within said trenches wherein said oxidation mask prevents oxidation of said polysilicon layer;

thereafter removing said oxidation mask;

depositing a trench oxide layer overlying said liner oxide layer and filling said trenches wherein said trench oxide layer comprises high density plasma silicon dioxide; and

polishing down said trench oxide layer and said polysilicon layer stopping at said silicon nitride layer wherein said polishing down is by a chemical mechanical polish having a polishing selectivity of oxide to polysilicon to nitride of 4:100:1 wherein said trench oxide layer takes on a concave formation when said polysilicon layer is polished and wherein after said all of said polysilicon layer is removed an overpolishing flattens said trench oxide layer to complete said shallow trench isolations in the manufacture of said integrated circuit device.

25. The method according to Claim 24 wherein said silicon nitride layer is deposited by chemical vapor deposition to a thickness of between about 800 and 2000 Angstroms.

26. The method according to Claim 24 wherein said polysilicon layer is deposited by chemical vapor deposition to a thickness of between about 500 and 1000 Angstroms.

27. The method according to Claim 24 wherein said oxidation mask comprises silicon nitride deposited by chemical vapor deposition to a thickness of between about 200 and 800 Angstroms.

28. The method according to Claim 24 wherein said step of oxidizing said silicon semiconductor substrate forms said liner oxide layer having a thickness of between about 100 and 300 Angstroms.

29. The method according to Claim 24 wherein said step of removing said oxidation mask comprises a wet etch before said step of depositing said trench oxide layer.

30. The method according to Claim 24 wherein said oxidation mask is removed during said polishing down process.

31. The method according to Claim 24 wherein said chemical mechanical polishing uses a slurry comprising

one of the group of: the combination of $NH_4OH$, silica abrasive, and de-ionized water and the combination of potassium hydroxide, silica abrasive, and de-ionized water; and wherein said chemical mechanical polishing process pad comprises polyurethane.